

**What is claimed is:**

1        1. A clock skew indicating apparatus comprising:  
2            a detection circuit for receiving as input first and  
3                second clocks and generating as output a compare  
4                signal; and

5            a sampling circuit, according to said compare signal,  
6                for asserting an output signal indicative of skew  
7                existing between said first and said second  
8                clocks.

1        2. The apparatus as recited in claim 1 wherein said  
2        first clock is transmitted with a differential signaling  
3        scheme.

1        3. The apparatus as recited in claim 2 further  
2        comprising a first differential-to-single-ended converter  
3        receiving said first clock, for providing said detection  
4        circuit with a version of said first clock converted into a  
5        single-ended signaling scheme.

1        4. The apparatus as recited in claim 3 wherein said  
2        second clock is transmitted with the differential signaling  
3        scheme.

1        5. The apparatus as recited in claim 4 further  
2        comprising a second differential-to-single-ended converter  
3        receiving said second clock, for providing said detection  
4        circuit with a version of said second clock converted into  
5        the single-ended signaling scheme.

1       6. The apparatus as recited in claim 1 wherein the  
2 width of said compare signal generated by said detection  
3 circuit is substantially proportional to an amount of said  
4 skew between said first and said second clocks.

1       7. The apparatus as recited in claim 6 wherein said  
2 sampling circuit samples said compare signal at a  
3 predetermined frequency such that said output signal is set  
4 to indicate the amount of said skew between said first and  
5 said second clocks.

1       8. The apparatus as recited in claim 7 further  
2 comprising a phase-locked loop for providing said sampling  
3 circuit with a reference clock running at said predetermined  
4 frequency.

1       9. An apparatus for indicating clock skew within  
2 integrated circuits (ICs) of a system, comprising:  
3            a first IC chip operating on a first clock and  
4            providing as output said first clock; and  
5            a second IC chip operating on a second clock,  
6            comprising:  
7              a detection circuit for receiving as input said  
8              first and said second clocks and generating  
9              as output a compare signal; and  
10             a sampling circuit, according to said compare  
11             signal, for asserting an output signal  
12             indicative of skew existing between said  
13             first and said second clocks;

14               wherein the width of said compare signal is  
15               substantially proportional to an amount of  
16               said skew between said first and said second  
17               clocks.

1               10. The apparatus as recited in claim 9 wherein said  
2       first IC chip comprises:

3               a control pin receiving an enable signal external to  
4               said first IC chip; and  
5               an output buffer coupled to receive said first clock,  
6               for outputting said first clock under control of  
7               said enable signal.

1               11. The apparatus as recited in claim 9 wherein said  
2       first clock is transmitted with a differential signaling  
3       scheme.

1               12. The apparatus as recited in claim 11 wherein said  
2       second IC chip comprises a first differential-to-single-  
3       ended converter receiving said first clock, for providing  
4       said detection circuit with a version of said first clock  
5       converted into a single-ended signaling scheme.

1               13. The apparatus as recited in claim 12 wherein said  
2       second clock is transmitted with the differential signaling  
3       scheme.

1               14. The apparatus as recited in claim 13 wherein said  
2       second IC chip further comprises a second differential-to-  
3       single-ended converter receiving said second clock, for  
4       providing said detection circuit with a version of said

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5 second clock converted into the single-ended signaling  
6 scheme.

1 15. The apparatus as recited in claim 9 wherein said  
2 sampling circuit samples said compare signal at a  
3 predetermined frequency such that said output signal is set  
4 to indicate the amount of said skew between said first and  
5 said second clocks.

1 16. The apparatus as recited in claim 15 wherein said  
2 second IC chip comprises a phase-locked loop for providing  
3 said sampling circuit with a reference clock running at said  
4 predetermined frequency.